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# APPLYING PARAMETRIC TEST PATTERNS FOR HIGH PIN COUNT ASICs ON LOW PIN COUNT TESTERS

## Abstract

Disclosed is an integrated circuit chip test apparatus that has a module test fixture having contact pads that are adapted to make contact with signal input/output pins on an integrated circuit chip being tested. An intermediate banking box is connected to the module text fixture and a tester is connected to the intermediate banking box. The tester includes at least one bank of channels there are more pins on the integrated circuit chip than there are channels in the tester. The intermediate banking box includes switches that are connected between the contact pads and the channels. The switches are adapted to selectively connect a subset of the contact pads to the channels to connect the tester to a subset of pins, thereby allowing the tester to test a portion of the integrated circuit that corresponds to the subset of pins.